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A Novel Approach to Image Moment Computation for Sonar Image Registration in Underwater Vehicle Autonomy

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ABSTRACT

Sonar image registration presents challenges due to its unique characteristics and real-time application demands. Sonar imagery, characterized by lower resolution and higher noise levels compared to optical images, lacks distinct features, complicating traditional detection methods. Moreover, computational complexity escalates with higher-order moments and larger image sizes. In real-time contexts like underwater vehicle autonomy, rapid and efficient moment computation is vital for timely decision-making and navigation. Overcoming these obstacles necessitates innovative hardware structures and parallel processing techniques. Building upon our previous study, where we introduced a systolic array and pipeline structure for high-order moment computation in grayscale images, this paper introduces the Parallel and Comparator-based Structure (PCS) to accelerate moment calculation for sonar image registration. By strategically relocating adders and integrating power cores, compressors, and adder units, PCS achieves streamlined computation with fixed latency. Experimental results demonstrate significant speed enhancements, positioning PCS as a promising solution for real-time underwater image processing.

1. Introduction

The development of new technologies, the refinement of sensor capabilities, and the continuous evolution of research in marine robotics have catalyzed the emergence of various underwater autonomous applications, including the manipulation and inspection of underwater structures and oil pipelines [1]. Despite notable strides, the realization of truly autonomous functionalities in underwater robotics remains somewhat constrained. These autonomous capabilities still heavily depend on precise environmental models and pre-programmed operations for their execution [2].
Within the realm of underwater robotics, image moments assume a pivotal role in facilitating tasks such as manipulation and inspection of underwater structures and oil pipelines. Serving as mathematical descriptors, image moments encapsulate critical properties of an image, including its centroid, area, and orientation. These descriptors furnish invaluable insights into the shape, size, and orientation of objects within the underwater milieu, thus proving indispensable for autonomous applications [3].
In manipulation tasks, image moments play a fundamental role in accurately detecting and localizing objects of interest, such as underwater structures or components of oil pipelines. Through the meticulous analysis of captured image moments, robotic systems can precisely ascertain the position and orientation of these objects, thereby facilitating effective manipulation maneuvers.
Similarly, in inspection tasks, image moments serve as vital tools in identifying anomalies or damages on underwater structures or pipelines. By comparing the moments of captured images with reference models or predefined criteria, robotic systems can discern deviations or irregularities, signaling potential areas of concern warranting further inspection or maintenance [4]. Furthermore, in the context of underwater applications, particularly in the inspection of structures and pipelines, the importance of image moments for accurate sonar image registration cannot be overstated [5]. These mathematical descriptors, adept at summarizing image properties, prove invaluable in tasks where visibility is limited and images are beset by noise. Consequently, the development of innovative methods for computing image moments tailored for sonar images holds promise for enhancing the accuracy and robustness of image registration processes. Such advancements are poised to augment the capabilities of autonomous underwater vehicles, particularly in tasks necessitating precise image alignment and localization.

2. Sonar Image Registeration

In contrast to optical images, which boast intricate textures, sonar images are simpler and cannot rely on robust point feature detectors [6]. Common algorithms used for describing optical features, such as SURF and SIFT, are unstable and unsuitable for sonar image analysis [7]. However, due to their visual simplicity, sonar images often exhibit well-defined geometric shapes. Sonar image registration typically utilizes Hu image moment calculation, facilitating the identification of clear geometric shapes [8]. All vehicle perceptions are translated into neurons known as local view cells. To extract reliable shapes from sonar images, preprocessing steps involving Gaussian and median filtering are applied to enhance shape clarity. Subsequently, the images are thresholded to convert them into binary format, followed by the derivation of image contours through the detection of points with high gradient.

The moment of a shape, denoted as M_{pq}, is calculated by summing the weighted intensities of its pixels.

$$M_{pq} = \sum_{x=1}^{m} \sum_{y=1}^{n} x^p y^q f(x,y) \qquad x \leq m, y \leq n \qquad (1)$$

Where, f(x, y) represents the binary representation of the shape. Our feature representation involves computing the seven Hu moments, initially introduced by Hu in 1962, for each shape. These Hu moments exhibit invariance to rotation, translation, and scale, making them robust descriptors for characterizing shapes.

It is crucial to emphasize the significance of speed in moment calculation for sonar image registration. Given the real-time nature of many underwater applications, such as navigation, inspection, and exploration, rapid processing of sonar images is essential for timely decision-making and effective operation of autonomous underwater vehicles (AUVs) [9]. By swiftly computing image moments during the registration process, AUVs can accurately and efficiently localize themselves in the underwater environment, enabling them to navigate safely and perform tasks effectively. Additionally, faster moment calculation enhances the responsiveness of AUVs to dynamic changes in their surroundings, ensuring agile and adaptive behavior in challenging underwater conditions. Therefore, the speed of moment calculation directly impacts the overall performance and reliability of sonar-based navigation and inspection systems deployed in underwater robotics.

Raffaitin et al. developed a hardware-based shape recognition system utilizing the NLM filter and Hu's moments, optimized for FPGA implementation [10]. They modified the NLM filter for FPGA simplicity and employed two finite state machines to compute Hu's moments and the NLM filter. Their study highlights the superior speed of hardware implementation compared to software-based approaches, especially in real-time image moment computation.

Watanabe et al. introduced a parallel extraction architecture designed to extract information from multiple objects efficiently [11]. Their proposed architecture was implemented in FPGA and validated to operate correctly. This system excels in extracting ample information from images, even when real-time processing at high-frame rates is demanded, making it highly beneficial for a wide range of applications.

Iwashita et al. presented the design of an image-moment sensor, starting with the theory behind moment calculation and proposing a variable-length pipeline for acceleration [12]. They implemented a 128 × 128 pixel sensor, reducing circuit area by sharing processing elements. Experimental evaluation confirmed its functionality. These sensors offer compact size, affordability, high resolution, sensitivity, and fast statistical calculation, making them valuable for real-time applications like robot systems, factory automation, and human interfaces.

We have recently introduced a novel structure utilizing systolic arrays and pipelines to compute high-order two-dimensional moments in grayscale images [13]. Each moment processor element (MPE) consists of adder, exponentiation, and multiplication units. The control unit receives data f(x, y) from the camera and transmits it along with relevant x and y values to each cell. When multiple MPEs are connected sequentially, they form a systolic array, with each cell responsible for processing specific portions of the image data. Figure 1 illustrates a structural arrangement comprising three MPE cells.

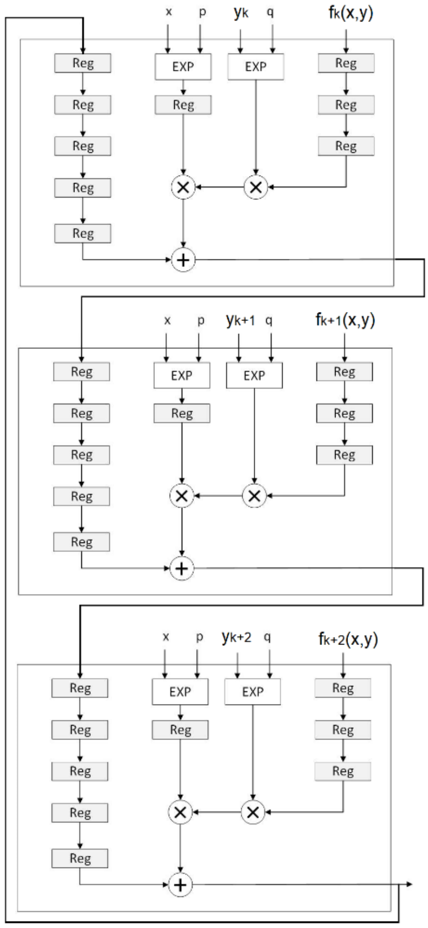


Figure 1. Systolic structure composed of three MPEs

4. Parallel Comparator-Based Structure (PCS)

By reconfiguring the systolic structure and relocating the adders to the exterior of the cells, a new design is proposed with fixed latency, regardless of the cell count. This innovative structure, termed Parallel and Comparator-based Structure (PCS), operates in parallel and employs a comparator for its functionality. Illustrated with nine cells, the PCS design is elucidated as follows.

Figure 1 illustrates the overall PCS structure. Power cores (PCs) perform computations in the form of $x^p y^q f(x, y)$ over five clock cycles, resulting in nine 18-bit numbers for subsequent addition. To expedite the summation process, a compressor is integrated. To ensure uniform input to the compressor, a comparator unit selects the largest representation among the nine numbers and adjusts the mantissa of each number accordingly. The revised mantissas feed into the 81-20 compressor unit, as depicted in Figure 3, which comprises nine 15:2 comparators and a 7:3 comparator. Each 15:2 comparator provides seven single-bit outputs, directing to the next 15-2 compressor. Figure 5 depicts the structure of the 7:3 comparator, while Figure 9 illustrates the internal configuration of a 15:2 comparator. With 22-bit outputs, the compressor unit pairs outputs for addition, facilitated by an 18-bit floating-point number adder, and the sum is then directed to the accumulator (ACC) input.

Importantly, the latency of the PCS structure remains fixed at 15 clock cycles, in contrast to the systolic structure, where latency equals the clock pulse period multiplied by (1 plus the number of cells times 5). Therefore, for a nine-cell structure, the systolic latency totals 50 clock cycles.

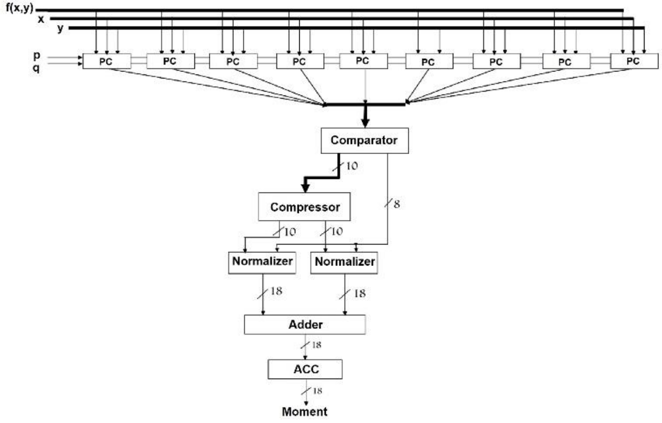


Figure 2. Parallel Comparator-Based Structure (PCS)

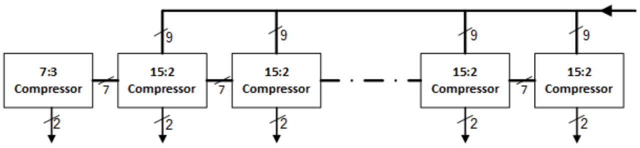


Figure 3. Architecture of 81: 20 Compressor

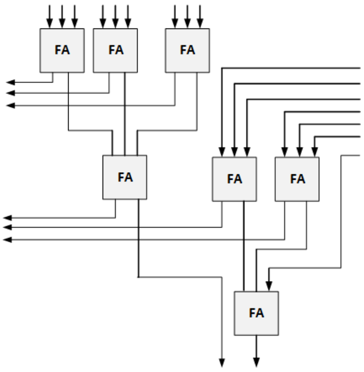


Figure 4. Design of 15:2 compressor

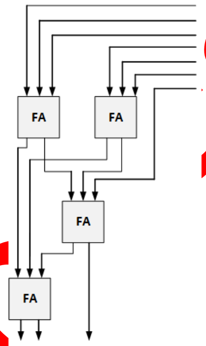
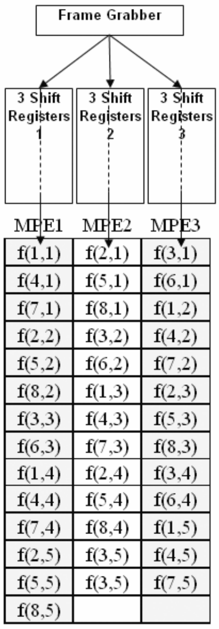


Figure 5. Structure of 7:3 compressor

4. 1 Shift Register Optimization for Parallelization

In the parallelization method, it is crucial for information to enter the cells simultaneously. To achieve this, the image information needs to be stored in a large number of 18-bit shift registers before the structure commences its operations. Consequently, shift register is essential before each cell, corresponding to the rows of the image. As the image dimensions and the number of Computer Elements (CE) cells increase, the required number of shift registers and constants also increase linearly. This leads to an increase in latency time and power consumption. Latency time refers to the duration needed to store the information of all the pixels of a column in the corresponding shift register. In the synchronous mode targeted in this article, all units within the structure calculate the output value on the rising edge of the clock pulse. To mitigate the number of shift registers and reduce latency, a method depicted in Figure 6 is proposed. In this scenario, the required number of shift registers becomes independent of the image dimensions and is n_{MPE}^2, where n_{MPE} represents the number of Moment Processor Elements (MPEs). This approach enables the calculation of the expression for each pixel of the image in one clock cycle, with the information of each pixel entering the system on the rising edge of the clock pulse. Consequently, the incubation time of the entire structure can be calculated, as indicated by Eq. 2, where n_{MPE} denotes the number of MPEs, m signifies the number of image rows, and T represents the period of the clock pulse. Notably, the reduction in latency time of the proposed method becomes more pronounced with an increase in m, as depicted in Figure 10.

$$Latency = Tn_{MPE}^2 + 5T(n_{MPE} + 1) = 5Tn_{MPE}(n_{MPE} + 1) \quad (2)$$



MPE1	MPE2	MPE3
f(1,1)	f(2,1)	f(3,1)
f(4,1)	f(5,1)	f(6,1)
f(7,1)	f(8,1)	f(1,2)
f(2,2)	f(3,2)	f(4,2)
f(5,2)	f(6,2)	f(7,2)
f(8,2)	f(1,3)	f(2,3)
f(3,3)	f(4,3)	f(5,3)
f(6,3)	f(7,3)	f(8,3)
f(1,4)	f(2,4)	f(3,4)
f(4,4)	f(5,4)	f(6,4)
f(7,4)	f(8,4)	f(1,5)
f(2,5)	f(3,5)	f(4,5)
f(5,5)	f(3,5)	f(7,5)
f(8,5)		

Figure 6. Proposed method for reduced shift register requirement and latency time

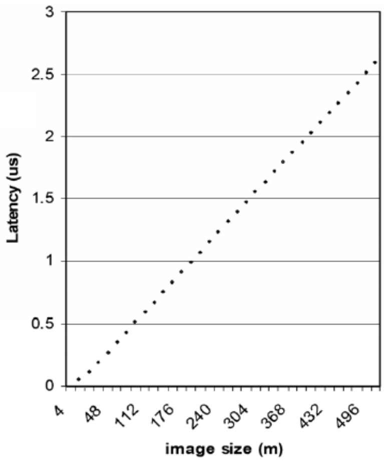


Figure 7. Effect of image size on latency reduction

5. Simulation Results

The physical characteristics of the moment computation structure were analyzed by synthesizing them with the Nangate 45nm open cell library using the Synopsys Design Compiler. Power consumption was estimated using the Synopsys power analysis tool, based on a VCD file generated from post-synthesis simulations with 100,000 random inputs. All comparisons were conducted post-synthesis at the block level, following ASIC designers' practices in thoroughly assessing building blocks for potential integration into future chips.

Table 1 compares various architectures, including the proposed approach, in terms of speed, power consumption, and area. The comparison of different architectures reveals varying trade-offs in terms of performance, power consumption, and area utilization. While Architecture [14] and [15] exhibit relatively lower transistor counts and smaller areas, they sacrifice speed and maximum moment order compared to Architecture [13] and PCS. Architecture [13] demonstrates exceptional speed and maximum moment order but at the cost of higher power consumption and a larger area footprint. Notably, the PCS architecture stands out for its impressive speed and maximum moment order, surpassing even Architecture [13], albeit with a trade-off of higher power consumption and a larger area requirement. This indicates that PCS offers significant performance enhancements suitable for demanding applications, although it necessitates careful consideration of power and area constraints. Overall, the choice between architectures depends on the specific requirements and priorities of the application, balancing performance with power and area considerations.

Table 1. Comparative performance analysis of various structures

Architecture	[14]	[12]	[15]	[13]	PCS
Max Moment Order	16	10	18	14	14
Transistor count	43894	143253	639804	543251	1167989
Speed (Gbit/s)	86.481	32.215	92.285	618.243	1060.286
Speed (frame/s)	45.277	25.568	84.237	954.012	1623.012
Power (mw)	254.863	185.657	19.586	3.254	5.018
Area (mm^2)	0.218	0.521	0.657	0.734	2.308

6. Conclusion

The primary objective of this paper was to explore novel architectural designs for moment computation in sonar image registration, aiming to enhance speed and efficiency. Through rigorous analysis and comparison, we have evaluated several architectures, culminating in the development of the Parallel and Comparator-based Structure. Our findings reveal that PCS offers significant advancements in performance metrics, boasting impressive values for speed and maximum moment order. Specifically, PCS achieves a maximum moment order of 14, outperforming other architectures. Additionally, with a speed of 1,623.012 frames per second and a transistor count of 1,167,989, PCS demonstrates remarkable efficiency. While PCS incurs a slightly higher power consumption of 5.018 mW and occupies a larger area of 2.308 mm2, these trade-offs are outweighed by its unparalleled speed and computational capabilities. In essence, the results of this study highlight the potential of innovative hardware design approaches, such as PCS, in advancing the capabilities of autonomous underwater systems. Looking ahead, further optimization and refinement of PCS hold promise for revolutionizing underwater vehicle autonomy and related applications, paving the way for safer and more efficient operations in marine environments.

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